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U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10014949	10/26/2001	257	25	2811	S RAO

**APPLICANTS: Yamamoto Makoto; Iwabuchi Akio;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN P2001-128187 04/25/2001

PG-PUB DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	44471-265522 (13700)
Verified and Acknowledged Examiner's initials		

TITLE : Lateral transistor having graded base region, semiconductor integrated circuit and fabrication method thereof

U S DEPT OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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